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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/421,322 | 10/18/1999 | HIROYUKI OI | PM-264817/OS | 3971 |

7590 03/15/2002

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| EXAMINER |
|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 03/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

| Application No. | Applicant(s) |
|---|---|
| 09/421,322 | Oi et al. |
| **Examiner** | **Art Unit** |
| George C. Eckert II | 2815 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) X Responsive to communication(s) filed on Dec 27, 2001 .

2a) X This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

**Disposition of Claims**

4) X Claim(s) 1, 3, 5, 6, and 9 is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) X Claim(s) 1, 3, 5, 6, and 9 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claims _____ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are objected to by the Examiner.

11) X The proposed drawing correction filed on Dec 27, 2001 is: a) ☒ approved b) ☐ disapproved.

12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119**

13) X Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) X All b) Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____ .
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

**Attachment(s)**

15) Notice of References Cited (PTO-892)

16) Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's amendment dated December 27, 2001 in which claims 2, 4, 7 and 8 were canceled, claims 1, 3, 5 and 6 were amended and claim 9 newly added has been entered of record.

### *Drawings*

2. The corrected or substitute drawings were received on December 28, 2001. These drawings are acceptable.

### *Specification*

3. Objection to the disclosure is overcome by applicant's amendment.

### *Claim Objections*

4. Objection to claims 6 and 8 are overcome by applicant's amendment.

### *Claim Rejections - 35 U.S.C. § 112*

5. Rejection of claims 3, 6 and 8 under 35 U.S.C. 112, second paragraph, are overcome by applicant's amendment.

### *Claim Rejections - 35 U.S.C. § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

### *Claim Rejections - 35 U.S.C. § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,420,064 to Okonogi et al. Okonogi et al. teach, with reference to figures 2 and 3A-E, a dielectrically separated wafer having a plurality of dielectrically separated monocrystalline silicon islands 11a (col. 3, lines 10-11), mutually defined by a dielectrically separating oxide film 13 on the surface of the wafer, wherein the dielectrically separated islands 11a comprise:

a high concentration impurity layer 12 (col. 3, lines 27-29) formed on the bottom of the islands; and

a low concentration impurity layer (the remainder of 11a) having an identical conductivity (n-, col. 3, lines 21-24) laminated on the high concentration layer.

With regard to claim 5, Okonogi et al., with reference to figures 2 and 3A-E, a dielectrically separated wafer having a plurality of dielectrically separated monocrystalline silicon islands 11a, insulated by a dielectrically separating oxide film 13 on the wafer surface, the dielectrically separated wafer comprises a surface between one dielectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat (see figure 3E for example which shows the area between islands 11a as flat).

7. Claims 3, 6 and 9 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Okonogi et al. With regard to claim 3, Okonogi et al. teach a dielectrically separated wafer having a polysilicon layer 14 and a plurality of polysilicon islands mutually separated by a dielectrically separating oxide film 13 formed on the surface of the polysilicon layer (those regions of polysilicon layer 14 which, in figure 3E for example, are shaped as triangles) wherein:

the polysilicon layer is formed on the dielectrically separating oxide film 13 by a high temperature method (col. 3, lines 34-37).

Regarding the limitation that the polysilicon layer has a seed layer grown by low temperature CVD and a polysilicon layer grown by high temperature CVD, these limitations are considered processing limitations which do not structurally differentiate over Okonogi et al. and

are thus considered anticipated by Okonogi et al. In the alternative, the limitation is considered merely an obvious processing variant over that taught by Okonogi et al., is considered within the skill of a mechanic in the art and is an obvious choice depending on the working limitations available to the manufacturer (e.g., if low temperature processes are required to avoid migration of dopants in other areas within the wafer).

With regard to claims 6 and 9, as discussed above Okonogi et al. teach the limitations of claim 1 and teach or make obvious the limitations of claim 3. Okonogi et al. did not expressly disclose that a flatness on the surface of the dielectrically separated islands is less than 0.2 μm when measured by a stylus-profilometer. However, this limitation is also considered either taught by Okonogi et al. or, in the alternative, obvious over the same. That is, Okonogi et al. teach that the wafer is "abraded and polished" (col. 3, lines 45-49) to form the islands. As such, it is considered inherent that the polishing will create a surface having no difference between the maximum and minimum values of flatness. In the alternative, it is considered obvious that the surface of the device of Okonogi et al. would be formed to have a flatness as instantly claimed. Though Okonogi et al. do not expressly disclose any value of a surface roughness, it is considered within the skill of a mechanic in the art to minimize any surface roughness as motivated by the relationship, known in the art, between surface roughness and complications of processing subsequent layers (alignment issues, planarity issues affecting wiring parameters, etc.). Therefore, claims 6 and 9 are considered either inherent or obvious over that taught by Okonogi et al.

***Response to Arguments***

8. Applicant's arguments filed December 27, 2001 have been fully considered but they are not persuasive. Applicant begins by arguing that "Okonogi does not disclose or suggest a high concentration impurity layer formed on the bottom of the islands and/or a low concentration impurity layer having an identical conductivity laminated on the high concentration layer." (See applicant's response, page 4). However, this argument simply ignores the straightforward teaching of Okonogi. Specifically, Okonogi teaches, with reference to figure 3E, a high concentration layer 12 formed on the bottom of the monocrystalline island 11a. Okonogi further teaches that the layer 12 is doped n+ (col. 3, line 31) which is the same conductivity as the island 11a formed from layer 11 (n-, col. 3, line 22-23). And, as stated in the rejection, the layer 11a reads on the limitation of the low concentration impurity layer.

Applicant continues arguments by stating that "layer 12 referred to, by the Examiner, as 'the high concentration impurity layer' is merely an n+-type layer." This argument seems to respond to itself. That is, an n+-type layer -the layer taught by Okonogi- *is* a high concentration impurity layer. The "+" symbol, as used by Okonogi and known in the art, designates a *high* concentration. Moreover, that a layer is designated as n-type indicates that *impurities* have been added to the otherwise intrinsic silicon. As such, the argument that Okonogi's n+-type layer is not a "high concentration impurity layer" is not persuasive.

Similarly, Applicant argues that the layer 11a of Okonogi does not read on the limitation of "a low concentration impurity layer" because Okonogi teaches that 11a is an island like

monocrystalline silicon film. However, Okonogi teaches that layer 11a is formed from n-type monocrystalline film which *is* a "low concentration impurity layer." As taught by Okonogi, layer 11a is ultimately formed from layer 11 and layer 11 is an n-type, monocrystalline silicon substrate (col. 3, lines 24-26). Applicant also argues that the layer 11a of Okonogi is not "laminated" as is the layer of the instant invention. However, the use of this term merely indicates one layer over another. If Applicant is instead suggesting that the limitation should be read as a processing limitation, Applicant is again reminded that a processing limitation is not sufficient for patentability if the final structure is taught in the art. Here, Okonogi has taught the final structure as claimed.

With regard to claim 5, Applicant argues that Okonogi has not taught the device wherein the dielectrically separating layer is flat and refers to figures 2, 1E and 3E of Okonogi. However, this argument ignores the teaching of Okonogi, specifically column 3, lines 45-49. There, Okonogi teaches that the device of figure 3D is abraded and polished with oxide layer 13 being exposed to the polishing. Because the surface of oxide layer 13 is exposed to the polishing step, the top of the oxide will be flat. That the figures may not precisely show such flatness is not sufficient to ignore the specific teaching and explanation provided by Okonogi.

Claims 3, 6 and 8 (now 9) were rejected using a 102/103 rejection as they recite processing limitations which are either inherent or obvious in the device of Okonogi. Applicant argues that the layer 14 taught by Okonogi does not read on the instant limitation as it lacks the characteristics of the polysilicon layer of the instant invention. However, this is merely a

conclusion by Applicant without support. No evidence has been provided which substantiates that a different final product is produced by Applicant from that produced by Okonogi. Similarly, the limitation of a specific surface flatness is merely argued by its advantage. Nothing has been shown which indicates that the final device of Okonogi does not anticipate the instantly claimed invention. Therefore, these arguments are not persuasive.

***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GEORGE C. ECKERT II
PATENT EXAMINER

GCE
March 13, 2002